

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

5 1-7 (cancelled).

8 (currently amended): A power supply voltage switching circuit for selecting a power supply voltage for an integrated circuit according to a first control signal, the circuit comprising:

10 a high ~~voltage power auto~~ selecting module for automatically generating an ~~output voltage intermediate voltage~~ according to a higher one of a voltage output by a ~~first power first outer power pin~~ and a ~~voltage output by a second power second outer power pin~~ which are directly connected to the high power auto selecting module at the same time without additional circuits or transistors, the high ~~voltage power auto~~ selecting module comprising:

15 a first transistor where a first terminal of the first transistor is electrically coupled to the ~~first power first outer power pin~~ without additional circuits or transistors, a second terminal of the first transistor is electrically coupled to an ~~output node intermediate node~~, and a gate of the first transistor is directly connected ~~electrically coupled~~ to the ~~second power second outer power pin~~ without additional circuits or transistors; and

20 a second transistor where a first terminal of the second transistor is ~~electrically coupled directly connected~~ to the ~~second power second outer power pin~~ without additional circuits or transistors, a second terminal of the second transistor is electrically coupled to the ~~output node intermediate node~~, and a gate of the second transistor is ~~electrically coupled directly connected~~ to the ~~first power first outer power pin~~ without additional circuits or transistors;

25 wherein the high ~~voltage power auto~~ selecting module selectively generates an ~~output voltage intermediate voltage~~ according to a higher one of the voltages ~~voltage~~ output by the ~~first power first outer power pin~~ and the ~~second power second outer power pin~~ which are directly connected to the first terminals and

gates of the first and second transistors at the same time, and
wherein the high power auto selecting module generates an intermediate
voltage automatically with no additional control signal;
automatically, and the first power and the second power are external power
5 sources;

a level shifting module electrically coupled to the high ~~voltage~~ power auto
selecting module for inputting the ~~output voltage~~ intermediate voltage as a power
supply of the level shifting module, for performing level shift on the first control
signal according to the ~~output voltage~~ intermediate voltage; and
10 a selecting switch module electrically coupled to the level shifting module, for
selectively outputting the voltage output by the ~~first power~~ first outer power pin or the
voltage output by the ~~second power~~ second outer power pin as the power supply
voltage of the integrated circuit according to the level-shifted first control signal.

15 9 (cancelled).

10 (previously presented): The circuit in claim 8, wherein the first transistor is a
p-type MOS transistor and the first terminal of the first transistor is a source and the
second terminal of the first transistor is a drain.

20 11 (previously presented): The circuit in claim 8, wherein the second transistor is a
p-type MOS transistor and the first terminal of the second transistor is a source and
the second terminal of the second transistor is a drain.

25 12 (previously presented): The circuit in claim 8, wherein the first transistor further
comprises a well and the well is electrically coupled to the second terminal of the first
transistor.

30 13 (previously presented): The circuit in claim 8, wherein the second transistor further
comprises a well and the well is electrically coupled to the second terminal of the
second transistor.

14 (currently amended): The circuit in claim 8, wherein when an absolute value of a difference between the voltages output by the ~~first-power~~ first outer power pin and the ~~second-power~~ second outer power pin is larger than a threshold voltage of the first and second transistors, and the output-voltage intermediate voltage is substantially the higher voltage output by the ~~first-power~~ first outer power pin and the ~~second-power~~ second outer power pin.

15 (currently amended): The circuit in claim 8, wherein when an absolute value of a difference between the voltages output by the ~~first-power~~ first outer power pin and the ~~second-power~~ second outer power pin is smaller than a threshold voltage of the first and second transistors, the output-voltage intermediate voltage is substantially the higher voltage output by the ~~first-power~~ first outer power pin and the ~~second-power~~ second outer power pin minus a junction voltage between the first terminal and the well of the first transistor or the second transistor.

16 (currently amended): The circuit in claim 8, wherein the level shifting module further performs level shift on a second control signal according to the output-voltage intermediate voltage, and the second control signal is complementary to the first control signal.

17 (currently amended): The circuit in claim 16, wherein the selecting switch module further comprises:

a third transistor where a first terminal of the third transistor is electrically coupled to the ~~first-power~~ first outer power pin, a second terminal of the third transistor is electrically coupled to a supply node, and the gate of the third transistor is electrically coupled to the level-shifted first control signal; and

a fourth transistor where a first terminal of the fourth transistor is electrically coupled to the ~~second-power~~ second outer power pin, a second terminal of the fourth transistor is electrically coupled to the supply node, and a gate of the fourth transistor is electrically coupled to the level-shifted second control signal;

wherein the selecting switch module generates the power supply voltage for the integrated circuit at the supply node according to the level-shifted first and second

control voltage.

18 (original): The circuit in claim 17, wherein the third transistor is a p-type MOS transistor and the first terminal of the third transistor is a source and the second
5 terminal of the third transistor is a drain.

19 (original): The circuit in claim 17, wherein the fourth transistor is a p-type MOS transistor and the first terminal of the fourth transistor is a source and the second
10 terminal of the fourth transistor is a drain.

20 (cancelled).

21 (currently amended): The circuit in claim 8 wherein the voltages output by the ~~first~~
~~power~~ first outer power pin and the ~~second power~~ second outer power pin are not
15 related to one another in any way.